PhD Project

Research project for the PhD curriculum “Electronics and Telecommunications”

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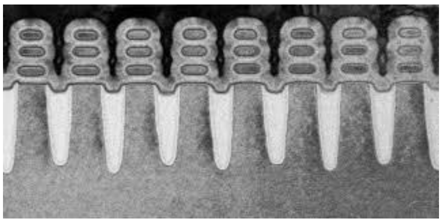
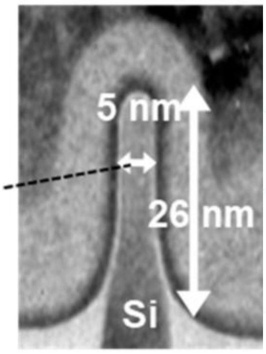
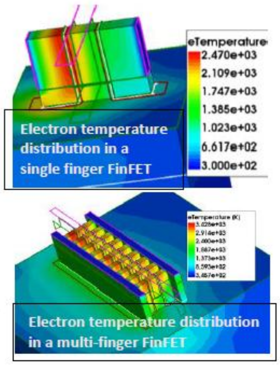


Title:
Alternative architectures and materials for nanoelectronic devices

Keywords: 3D MOSFET architectures, 2D- and Dirac materials, self-heating, noise and fluctuation phenomena, DC and RF MOSFET performance

Introduction:





Recent developments of nanoelectronic technologies make increasing use of alternative semiconductors of the IV-IV, III-V groups, and 2D materials, alternative high-k and low-k dielectrics and new device architectures (e.g. FinFET, stacked nanosheets, nanowire, and CFET) to improve device performance at the ultimate scaling limits exploiting, among other bosters, 3D integration solutions. Unfortunately, self-heating, noise, defects, and fluctuation phenomena hamper the device and circuit performance (both analog and digital, static and RF) at these so tiny dimensions. Furthermore, the Boltzmann tyranny impedes to achieve subthermal subthreshold swing (SS< 60 mV/dec) in the transfer characteristics of MOSFETs.

Proposed research activity and PhD thesis objectives:

The objective of the PhD thesis is to investigate by using TCAD tools, multiscale-multiphysics approaches and advanced in-house simulation models, how self-heating and defects influences the performance and the reliability of nano-electronic devices fabricated with advanced 3D architectures and alternative materials for the channel and/or the dielectric (including 2D and Dirac materials). The activity includes analysing the noise generation and fluctuation in the semiconductor and insulators due to traps and defect, as well as the influence of dynamic self-heating up to GHz frequencies, which pose a challenge to the realization of accurate RF circuits for the upcoming communication standards. These studies will be instrumental in benchmarking different technology options and to guide the layout of devices to minimize self- and cross-heating effects. The study should also lead to develop higher level Verilog-A models amenable to integration in circuit simulation frameworks for mixed analog/digital and RF circuit blocks. Comparison to experimental data provided by international partners is part of the activity.

Supporting research projects (and Department)

The activity will be carried out at the DIEF, Università degli Studi di Modena e Reggio Emilia and may include a stage at a partner institution in Europe

Connections with research groups, companies, universities.

Infineon Technlogies
NXP semicondutcors
IUNET Research Consortium (www.iunet.info)