Project description

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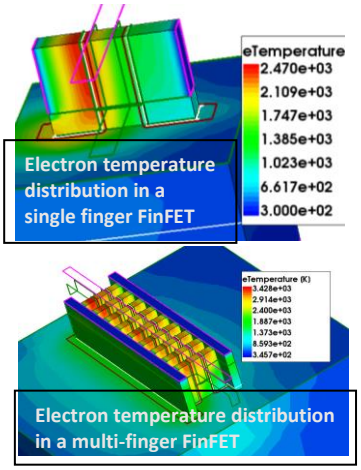

Title:
Nanosecond timescale self-heating effects in advanced FinFET and FDSOI nanoscale MOSFETs

Introduction:

Nanoscale FinFETs and FDSOI MOSFETs in modern CMOS technologies are expected to exhibit remarkable self-heating effects, because of difficult-to-downscale power area-density, circuit density, new materials, etc. Self-heating increases carrier scattering and reduces the mobility; as a result, both small core and large I/O transistor characteristics are dynamically distorted. Furthermore, reliability is degraded. The dominant thermal time constants for these processes are estimated in the deep sub-microsecond range and projected to reach the nanosecond level in the near future. Therefore, not only the static but also the small and large signal RF performance of the transistors is modified.

At the state of the art, these effects are poorly described at the lumped-element level, thus casting non-negligible uncertainty on the design of complex circuits where accuracy is important, e.g., RF design for WiFi and 6G modulation standards and ADC design in advanced technology nodes.

The main goal of the project is to elaborate compact, lumped-element models of device self-heating, suited to predict the device thermal time constant(s) and their scaling with device layout and dimensions.

Proposed research activity and thesis objectives:
The objective of the thesis is to investigate investigate the transient static and RF performance of a few modern MOSFET architectures by means of physics-based finite element simulations and comparison with experimental data on dedicated test structures. From the methodological point of view, advanced simulation tools and commercial TCAD (e.g., Synopsys SDevice), jointly with ad-hoc models developed in MATLAB or equivalent programming environment, will be used to study the nominal device performance, estimate the performance degradation induced by temperature rise, propose test structures and implement adequate characterization procedures to measure the thermal transients and calibrate the model. Compact models based on lumped elements, and possibly Verilog-A codes, will be developed to enable circuit- and mixed-mode device-circuit simulations of analog and digital blocks realized with these new technologies. Model parameters will be extracted from finite element simulations. Comparison to experimental data provided by international partners will be part of the activity.

Vision goals of the activity: The ultimate goal of the study is to investigate the impact of self-heating in RF circuits up to a few GHz. and to propose adequate characterization techniques, as well as measures to mitigate performance degradation. To this end, the following steps are envisioned: 1) to develop finite-element simulation models calibrated on DC, pulsed and RF measurements, suited to predict the self-heating of advanced devices for More Moore applications fabricated at the partner institutions; 2) to investigate by simulation the morphology, size and material dependence of the thermal resistances and capacitances for a few representative devices with single and multi-finger layout; 3) to couple the thermal and electrical lumped-elements device models in a circuit design model including self-heating effects; to use the model for circuit analysis including self-heating.

Supporting research projects (and Department)
The activity will be carried out at the DIEF, Università degli Studi di Modena e Reggio Emilia and may include a stage at NXP Semiconductors in The Netherlands.

Connections with research groups, companies, universities.
NXP Semiconductors, The Netherlands
Possible interaction with nanoelectronic research groups of the IUNET Consortium (www.iunet.info)