Project description

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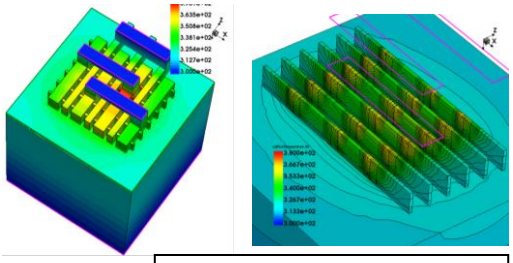
Title: Computational analysis of advanced devices and components for sustainable electronics



Electron temperature distribution in advanced multi-fin multi-finger

Introduction: Energy efficient electronic devices and components are critically important to design smarter products supporting the ecological transition toward a sustainable economy. In this respect, the material quality and the power dissipation in modern, densely packed and highly integrated electronic devices and components causes significant inefficiencies and poses increased design challenges. Effective reduction of defect concentrations and efficient removal of the heat is critical to maintain high electrical performances, fully leverage the advantages of (3D) integration and advanced packaging solution, ensure low noise, long term reliability and eventually enable the integration of smarter components into the systems. In this respect, future CMOS electronic technologies are expected to exhibit increasing self-heating effects and variability issues due to discrete traps, unless new solutions are found for materials' choice, quality, layouts, and self-correcting circuitry to mitigate adverse effects. At the microscopic level, self-heating increases carrier scattering and reduces the mobility, resulting in dynamic distortions of the transistor characteristics and hard to predict and optimize behavior. Numerous detrimental effects are known to be associated to traps and noise as well. The dominant time constants for these processes are heavily dependent on material and layout choices, and are projected to reach the nanosecond level in the near future. Therefore, both static, and small and large signal RF performance of transistors and circuits is modified. At the state of the art, these effects are poorly described at the lumped-element level, thus casting non-negligible uncertainty on the design of complex circuits and systems where accuracy is important, e.g., RF design for WiFi and 6G modulation standards and ADC design in advanced technology nodes. The complexity of the nowadays finFET, nanosheet and nanofork devices requires huge computational resources to be tackled at the FEM level.

The main goal of the project is to massively exploit HPC computational resources to elaborate FEM and compact, lumped-element models of device and component trap induced noise, variability and self-heating, suited to predict the thermal time constant(s) and their scaling with device layout and dimensions, and to exemplify the new methodologies on relevant use cases. Ultimately, the project will lead to physics-based models to support the design of advanced electronic components with improved performance, reliability, sustainability.

From the methodological point of view, advanced simulation tools and commercial TCAD (e.g., Synopsys SDevice), jointly with ad-hoc models developed, e.g., in MATLAB, will be used to study the nominal device performance, estimate the performance degradation due to traps and overtemperatures, propose test structures and implement adequate characterization procedures to measure the transients and calibrate the models. Parallelization and efficient use of HPC resources will be investigated to cope with the required multiscale-multiphysics problem. Compact models based on lumped elements or Verilog-A will be developed to enable efficient, strongly physics-based circuit- and mixed-mode device-circuit simulations of analog and digital blocks realized with these new technologies

Vision goal of the activity: The goal of the study is to contribute to optimal design of more energy efficient advanced electronic components in support of the ecological transition. To this end, the candidate will develop and disseminate new competences and tools on electro-thermal models for advanced electronic components in CMOS technology, suited to improve electronic design performance and reliability. The following steps are envisioned: 1) to develop HPC-based FEM simulation models, calibrated on DC, AC, pulsed and RF measurements, to predict the self-heating of advanced semiconductor device components; 2) to investigate by simulation the morphology, size and material dependence of the lumped element thermal resistances and capacitances; 3) to couple the thermal and electrical lumped-elements device models in a circuit design model including self-heating effects; 4) to use the model for circuit analysis and optimization.

Supporting research projects (and Department): The activity will be carried out at the DIEF, Università degli Studi di Modena e Reggio Emilia as part of the ECOSISTER spoke 6 PNRR project and includes a stage at NXP Semiconductors in The Netherlands.

Connections with research groups, companies, universities: Possible interaction with NXP Semiconductors, The Netherlands, nanoelectronic research groups of the IUNET Consortium (www.iunet.info), Applied Materials Italy and electronic components' companies will be pursued.